WHAT IS CLAIMED IS:

1. A multibit non-volatile memory cell structure comprising:

a semiconductor substrate of a first conductivity type;

first and second junction regions of a second conductivity type, said first and said second junction regions defining at least a portion of first and second bitlines, respectively; and

a select gate defining therein at least a portion of a wordline, which extends perpendicular to said first and said second bitlines, wherein read, write and erase functions for each cell involve only two polysilicon layers, and wherein each cell comprises at least two locations for storing a charge representing at least one bit.

2. A device according to Claim 1, wherein at least an edge of said first bitline is substantially collinear with an edge of one of said two locations for storing the charge, and at least an edge of said second bitline is substantially collinear with one of said two locations for storing the charge, and wherein the select gate separates said two locations for storing the charge.

3. A device according to Claim 2, wherein the charge storage locations comprise a vertical cross-section of uniform thickness.

4. A device according to Claim 3, wherein a first dielectric layer separates a first layer of said two polysilicon layers from said semiconductor substrate, and a second dielectric layer separates a second layer of said two polysilicon layers from said semiconductor substrate.

5. A device according to Claim 4, wherein said first and second charge storing locations comprise floating gates, and the charge is stored within said first polysilicon layer of each charge storage location.

6. A device according to Claim 5, further comprising first and second program gates formed parallel to said wordline within said second polysilicon layer, said first and said second program gates being overlapping with said first and said second charge storing locations, respectively.

7. A device according to Claim 5, wherein said first polysilicon layer is located

underneath said wordline.

8. A device according to Claim 4, wherein said first and second charge storage locations comprise program gates, and said first dielectric layer comprises a charge storing dielectric.

9. A device according to Claim 8, wherein said charge storing dielectric comprises an oxide having polysilicon nanocrystals or nitride, said nitride or polysilicon being capable of holding charge in selected regions thereof and said first polysilicon layer is configured as program gate.

10. A device according to Claim 9, wherein said second dielectric layer comprises a charge storing dielectric.

11. A device according to claim 10, wherein said charge storing dielectric of said second dielectric layer comprises a nitride or an oxide having polysilicon nanocrystals, said nitride or oxide being capable of holding charge in selected regions thereof.

12. A method of forming a multibit non-volatile memory cell structure comprising the steps of:

depositing a first polysilicon layer on a semiconductor substrate of a first conductivity type;

depositing and patterning a first hardmask layer to form at least a first hardmask region upon said first polysilicon layer;

depositing and anisotropically etching a second hardmask layer forming second hardmask spacers adjacent to said at least a first hardmask region;

selectively removing exposed parts of said first polysilicon layer;

removing said at least first hardmask region to expose the first polysilicon layer underneath said at least first hardmask region;

removing the exposed parts of said first polysilicon layer underneath said at least first hardmask region to form first and second polysilicon gates having an uniform thickness, one on each side of said at least first hardmask region;

removing said second hardmask spacers and exposing said first and second polysilicon gate; and

depositing and patterning a second polysilicon layer perpendicular to said first and second polysilicon gate to form a third polysilicon gate separating said first and said second polysilicon gate.

13. A method according to Claim 12 further comprising:

forming a first dielectric layer isolating said first polysilicon layer from said semiconductor substrate; and

forming a second dielectric layer isolating said second polysilicon layer from said semiconductor substrate.

14. A method according to Claim 13, wherein said first and second dielectric layers comprise oxide and said first and said second polysilicon gate form a floating gate.

15. A method according to Claim 14, further comprising forming in said second polysilicon layer first and second program gates that are parallel to said wordline, said first and said second program gates overlapping with said first and said second polysilicon gates, respectively.

16. A method according to Claim 13, further comprising the step of etching said first polysilicon layer to collinearly align at least an edge of said first polysilicon layer with an edge of said second polysilicon layer, after the step of depositing and patterning said second polysilicon layer.

17. A method according to Claim 13, wherein said first dielectric layer comprises a charge storing dielectric.

18. A method according to Claim 17, wherein said second dielectric layer comprises a charge storing dielectric.

19. A multibit non-volatile memory cell array comprising:

a plurality of memory cells arranged in an active area region as a matrix of rows and columns, each memory cell comprising:

a semiconductor substrate of a first conductivity type;

first and second junction regions of a second conductivity type, said first and said second junction regions forming at least a portion of first and second bitlines, respectively;

a select gate forming at least a portion of a wordline extending perpendicularly to said first and said second bitlines;

wherein read, write and erase functions for each cell involve use of only two polysilicon layers, and wherein each memory cell has at least two locations for storing a charge representing at least one bit.

20. A memory cell array according to Claim 19, wherein first and second program gates are formed in a first polysilicon layer, and further comprising a contact pad formed in the first polysilicon layer for each of said program gates, said contact pad for said program gate being alternately formed at opposite sides of the memory matrix.